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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,409	09/04/2001	Takehiro Shimizu	NITT.0039	1210

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,409	SHIMIZU ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5* is/are rejected.

7)☐ Claim(s) *4 and 6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation, IA-64 Application Developer's Architecture Guide, May 1999 (hereinafter referred to as Intel).

3. Referring to claim 1, Intel has taught a processor comprising:

a. a register file including a plurality of registers assigned with register numbers, each of the registers storing operand data (Page 7-1);

b. a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of the operand data (Page 7-137, padd);

c. a decoder for decoding a register designating field of an instruction code (Page 6-2, section 6.1.1, first bullet point, page C-17, Bits 13-26 comprise the register designating field.), said register designating field having a designating number stored therewith (page C-17, Bits 13-26 have register number r2 and register number r3 stored therewith.), said decoder further for generating signals designating register numbers based on the designating number of the register designating field (page 7-137, padd, page C-17, Signals designating register numbers r2 and r3 are generated.).

d. a control circuit for sending operand data stored in the registers corresponding to the designated register numbers to at least one of the operation pipes such that said at least one of the operation pipes executes in parallel the one kind of operation associated therewith on the operand data sent from the corresponding designated registers (page 7-137, padd).

4. Intel has not specifically taught said designated register numbers being consecutive according to the designating number of the register designating field. However, Yoshida has taught designated register numbers being consecutive according to a designating number of a register designating field (abstract, column 2, line 1-column 3, line 29) for the desirable purpose of effectively accessing multiple pieces of data at the same time (abstract, column 2, line 1-column 3, line 29). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the processor of Intel designate register numbers that are consecutive according to the designating number of the register designating field, as taught by Yoshida, for the desirable purpose of effectively accessing multiple pieces of data from the registers at the same time (abstract, column 2, line 1-column 3, line 29).

5. Referring to claim 2, Intel has taught a processor comprising:

a. a register file including a plurality of registers assigned with register numbers (Page 7-1);

b. a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of the operand data so as to generate operation result data (Page 7-137, padd);

c. a decoder for decoding a register designating field of an instruction code (Page 6-2, section 6.1.1, first bullet point, page C-17, Bits 13-26 comprise the register designating field.), said register designating field having a designating number stored therewith (page C-17, Bits 13-26 have register number r2 and register number r3 stored therewith.), said decoder further for generating signals designating register numbers according to the designating number of the register designating field, and the registers corresponding to the designated register numbers being designated for storing the operation result data (page 7-137, padd, page C-17, Signals designating register numbers r2 and r3 are generated.); and

d. a control circuit for sending the operation result data from at least one of the operation pipes to the corresponding designated registers (page 7-137, padd).

6. Intel has not specifically taught said decoder further for generating signals designating register numbers according to the designating number of the register designating field so as to be consecutive to each other. However, Yoshida has taught a decoder further for generating signals designating register numbers according to a designating number of a register designating field so as to be consecutive to each other (abstract, column 2, line 1-column 3, line 29) for the desirable purpose of effectively accessing multiple pieces of data at the same time (abstract, column 2, line 1-column 3, line 29). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the decoder of Intel generate signals designating register numbers according to the designating number of the register designating field so as to be consecutive to each other, as taught by Yoshida, for the desirable purpose of effectively

accessing multiple pieces of data from the registers at the same time (abstract, column 2, line 1-column 3, line 29).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prabhu, US Patent 6,463,525.

8. Referring to claim 3, Prabhu has taught a processor comprising:

a. a register file including a plurality of registers assigned with register numbers, each of the registers for storing at least one of operand data and operation result data (Abstract, Figures 1 and 2, element 40);

b. a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of the operand data so as to generate the operation result data (abstract, Figure 2, column 3, line 14-43, column 5, lines 45-56);

c. a first decoder for decoding a first register designating field of an instruction code (Figure 2, column 5, TABLE 2, fadd, d0 is inherently decoded.), said first register designating field having a first register designating number stored therewith (Figure 2, column 5, TABLE 2, d0), said first decoder further for generating signals designating source register numbers based on the first register designating number (Figure 2, column 5, TABLE 2, When d0 is decoded, signals for f0 and f1 are generated.);

d. a second decoder for decoding a second register designating field of the instruction code (Figure 2, column 5, TABLE 2, fadd, d2 is inherently decoded.), said second register designating field having a second register designating number stored therewith (Figure 2, column 5, TABLE 2, d2), said second decoder further for generating signals designating result register numbers based on the second designating register

number (Figure 2, column 5, TABLE 2, When d2 is decoded, signals for f2 and f3 are generated.); and

e. a control circuit for sending the operand data stored in source registers corresponding to the designated source register numbers to at least one of the operation pipes such that said at least one of the operation pipes executes in parallel the one kind of operation associated therewith on the operand data and for sending the operation result data obtained from the at least on operation pipe to result registers corresponding to the designated result register numbers (abstract, column 5, lines 45-56).

9. Prabhu has not specifically taught said first decoder further for generating signals designating source register numbers based on the first register designating number so as to be consecutive to each other and said second decoder further for generating signals designating result register numbers based on the second designating register number so as to be consecutive to each other. However, Yoshida has taught generating signals designating register numbers based on a register designating number so as to be consecutive to each other (abstract, column 2, line 1-column 3, line 29) for the desirable purpose of effectively accessing multiple pieces of data at the same time (abstract, column 2, line 1-column 3, line 29). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first decoder of Intel generate signals designating source register numbers based on the first register designating number so as to be consecutive to each other and the second decoder of Intel generate signals designating result register numbers based on the second designating register number so as to be consecutive to each other, as taught by Yoshida, for the desirable purpose of

effectively accessing multiple pieces of data from the registers at the same time (abstract, column 2, line 1-column 3, line 29).

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation, IA-64 Application Developer's Architecture Guide, May 1999 (hereinafter referred to as Intel).

11. Referring to claim 5, Intel has taught the processor according to claim 1, as described above. Intel has not specifically taught wherein the number of the plurality of registers is limited to the n-th power of 2n is a natural number, so as to reduce register selecting circuits. However, having the number of registers limited to the n-th power of 2 would maximize the efficiency of the wiring as none of the bit combinations would be wasted. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the number of the plurality of registers, as taught by Intel, be limited to the n-th power of 2 where n is a natural number, to thereby enable to reduce register selecting circuits, for the desirable purpose of maximizing the efficiency of the wiring as none of the bit combinations would be wasted.

Response to Arguments

12. Applicant's arguments with respect to claims 1-3 and 5 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

13. Claims 4 and 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100